AUTHOR(S): AHMED, K.H. and ABOUSHADY, A.A.

TITLE: Modified half-bridge modular multilevel converter for HVDC systems with DC fault ride-through capability.

YEAR: 2014

Publisher citation: AHMED, K.H. and ABOUSHADY, A.A. 2014. Modified half-bridge modular multilevel converter for HVDC systems with DC fault ride-through capability. In the Proceedings of the 40th annual conference of the IEEE industrial electronics society (IECON 2014), 30 October - 1 November 2014, Dallas, USA. New York: IEEE [online], pages 4676-4682. Available from: https://dx.doi.org/10.1109/IECON.2014.7049207.

Modified Half-bridge Modular Multilevel Converter for HVDC Systems with DC Fault Ride-Through Capability

K.H. Ahmed[+] and A.A. Aboushady[*]
[+]School of Engineering, University of Aberdeen, Aberdeen, UK
[*]Electrical and Control Engineering Department, Arab Academy for Science and Technology, Alexandria, Egypt

***Abstract*- One of the main challenges of voltage source converter based HVDC systems is DC faults. In this paper, two different modified half-bridge modular multilevel converter topologies are proposed. The proposed converters offer a fault tolerant against the most severe pole-to-pole DC faults. The converter comprises three switches or two switches and 4 diodes in each cell, which can result in less cost and losses compared to the full-bridge modular multilevel converter. Converter structure and controls are presented including the converter modulation and capacitors balancing. MATLAB/SIMULINK simulations are carried out to verify converter operation in normal and faulty conditions.**

I. INTRODUCTION

Nowadays, voltage source converter high voltage DC (VSC-HVDC) transmission system is a best candidate to meet DC electrical network developments and challenges due to its operational flexibility, such as provision of voltage to AC networks; operates independent of AC network strength, therefore suitable for connection of weak AC networks such as offshore wind farms [1-2]. Also it is suitable for multi-terminal HVDC network realization as active power reversal is achieved without change of DC link voltage polarity. A VSC-HVDC is resilient to AC side faults (no risk of commutation failure as with line commutating HVDC systems). However, vulnerability to DC side faults and absence of reliable DC circuit breakers capable of operating at high voltage restrict their application to point-to-point connection.

Currently there are two established approaches for the VSC-HVDC system construction namely, standard two-level converters and multilevel converters. The voltage source multilevel converters are classified as diode clamped, flying capacitor, cascaded (with isolated DC sources) and modular converters.

Modular multilevel converter (MMC) is an attractive alternative to conventional multilevel converters in medium/high voltage applications [3-5]. It provides a viable approach to construct a reliable and cost effective AC voltage with increased number of levels. It can potentially operate continuously under unbalanced conditions, capable of surviving symmetrical and asymmetrical AC faults without increasing the risk of system collapse and some topologies have DC fault management capability. As all VSCs it can independently control, active and reactive AC power and readily rides through AC disturbances. The most attractive feature is the modularity, since same basic modules are used in all projects, whereas only the number of module differs. However, this approach suffers from some drawbacks such as the need to manage the charge balance of the cell capacitors, and large number of switches (almost double). Also, the MMC cell capacitors experience the fundamental frequency current and must have high capacitances to limit cell voltage excursions.

There are two approaches to assist VSC-HVDC transmission systems to ride-through DC side faults. The first approach is to use a fast acting DC circuit breaker, with considerably high let-through current to tolerate the high DC fault discharge current that may flow in the DC side. This breaker must be capable of operating at high voltage and isolates temporary or permanent DC faults, plus have a relatively high current breaking capacity. The development of fast DC circuit breaker is in early stages. A prototype of 80-kV DC circuit breaker with DC current breaking capacity of 9 kA within 2ms has been proposed [6]. However, this proposal is inadequate, as the operating voltage of today VSC-HVDC transmission systems reaches 640 kV pole to pole with power handling capability of 1 GW.

The second approach is to use the converter stations with DC fault reverse blocking capability [7]. Each converter station must be able to block current flow between the AC and DC sides during a DC fault. Several converter topologies with this inherent feature have been proposed, including a full-bridge modular multilevel converter, an alternative arm modular multilevel converter, and a hybrid multilevel converter with ac-side cascaded full-bridge cells. However, the drawback is that a full-bridge converter has to be embedded in any of the above topologies to block the current. Full-bridge converter will not only add complexity and higher losses but also higher footprint and cost.

In this paper, two different modified half-bridge MMC topologies are proposed. In normal operating mode, the modified MMC is working like the conventional half bridge converter. During faults, the gate drive signals are inhibited and the converter cells are blocked. The current from the AC to DC side is zero thanks to the proposed topologies. The modified converter

has excellent DC fault-ride through capability like full-bridge MMC. The converter structure, control and operation are presented. A simulation study is carried out using MATLAB/SIMULINK to validate the proposed converter during normal and fault conditions.

II. Proposed Multilevel Converter

Modular multilevel converter is an alternative to conventional multilevel converters in medium/high voltage applications. Currently there are two main configurations, namely half-bridge and full-bridge modular converters. The converter leg consists of positive and negative arms. Each arm comprises a series chain of n-cells. Each sub module (cell) includes one capacitor, which will store energy for the converter instead of the conventional DC-link capacitor and several switches and diodes. Also there are interfacing inductors, which are used to limit the circulating current due to the imbalance voltage of the converter cells during the switching process. The arm inductor selecting is a crucial parameter MMC design. The criteria for designing the arm inductor are to suppress the circulating current including 2nd order harmonics, limit the fault current during DC faults and avoid the converter arm resonance between the arm inductor and cell capacitance. The arm inductor is typically selected within a range of 10to 15% to achieve the above criteria. This circulating current includes a second order harmonic component which not only deforms the arm currents, but also increase the sub module voltage ripples. The proposed topologies of one phase MMC for n+1 levels are shown in Fig 1. The two proposed topologies are different in the module structure.

The AC current of the converter is:

$$i_a = i_P + i_N \tag{1}$$

where i_P and i_N are the current flowing through the positive and negative arms respectively. For maximum utilisation of the MMC, capacitor voltage of each module V_C is:

$$V_C = \frac{1}{n} V_{DC} \tag{2}$$

where n is the number of cells per arm.
The DC-link voltage equals:

$$V_{DC} = V_P + V_N \tag{3}$$

where V_P and V_N are the maximum voltage sum of all the cascaded cells (2n) in positive and negative arms respectively. The instantaneous values of the sum of all cell voltages in upper and lower arm are $V_p(t)$, and $V_N(t)$ respectively, so the voltage inserted by the phase k for the upper and lower arms are:

$$V_P^k = m_P(t) V_P(t) \quad , \quad V_N^k = m_N(t) V_N(t) \tag{4}$$

where $m_P(t)$, and $m_N(t)$ are the upper and lower arm modulation indexes. They are determined by the number of cells inserted using the control circuit. By using KVL, the system dynamic equation is

$$V_a = -m_P(t) V_P - (R + \frac{d}{dt} L) i_P + \frac{V_{DC}}{2} \tag{5}$$

$$V_a = m_N(t) V_N - (R + \frac{d}{dt} L) i_N - \frac{V_{DC}}{2} \tag{6}$$

The cell capacitor design is significant, as the cell capacitor of MMC is carrying the load current and it represents the storage element for the converter instead of the DC-link capacitors. There is always a trade-off between cell voltage ripple requirements and capacitor size. The cell capacitor is typically selected so the cell ripple voltage is kept within a range of 10%. In order to achieve the above ripple limits, the energy stored in a module should be in the range of E_{module}=30–40 kJ/MVA (where MVA refers to the total converter rating) [8].

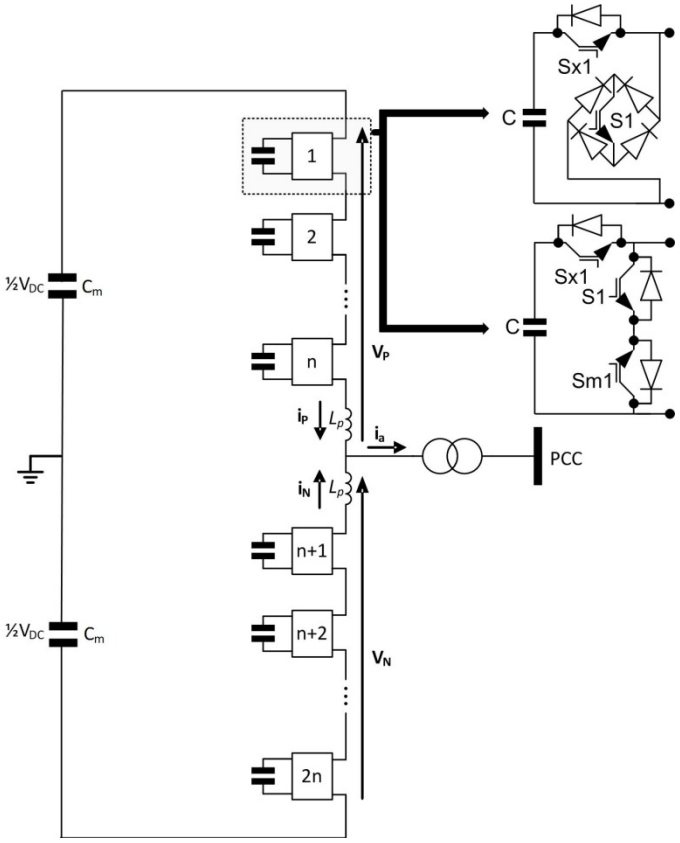


Fig.1. Single phase modular multilevel converter structure for n+1 level

A. Topology 1

Each module consists of one IGBT packs (IGBT plus free-wheeling diode), IGBT switch, four diodes and a capacitor. The two switches are operated exactly like one leg of a 2-level half bridge converter. When one of the switches is fired ON the other

switch will be OFF and vice versa. The operation of the modified half-bridge module is shown in the Table I during the ON (represented by state 1) and OFF (represented by state 0) states with different current directions. The third status is module blocking (both switches are off). This configuration isolates the module totally such as full-bridge MMC due to the existing of diodes.

A. Topology 2

In this topology, each module is consisted of three IGBT packs (IGBT plus freewheeling diode) and a capacitor. Here, a module like topology 1 has the capability to block the current flowing from the AC to the DC side during DC faults. However, the additional switch increases the semiconductor losses. Additional disadvantage is the converter station increases footprint. The operation of the modified half-bridge module is shown in Table I during the cell ON and OFF states with different current direction.

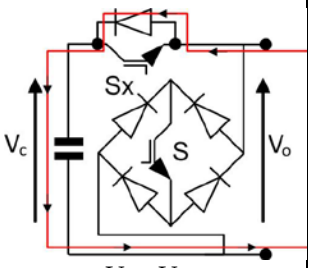
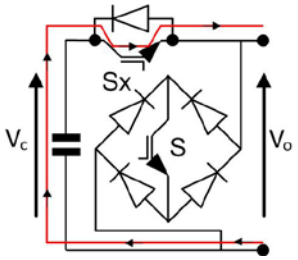
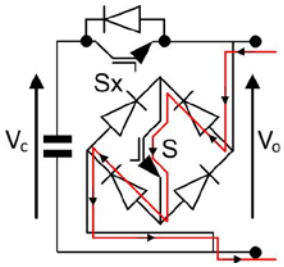
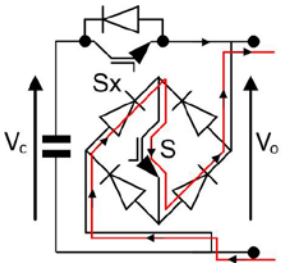
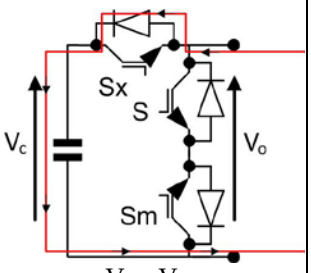
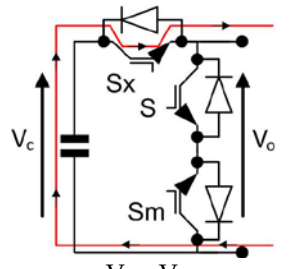
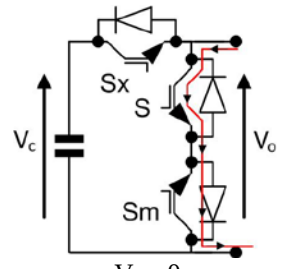
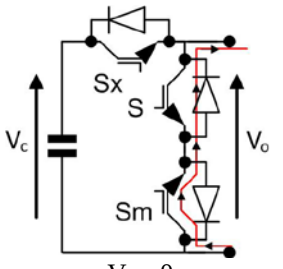
III. Converter Modulation

All modulation schemes aim to create a link, which has the same fundamental voltage-second average as a target reference waveform at any instant. The major difficulty with the different used techniques is those output signals contain unwanted harmonic components, which should be minimized.

Hence, for any common modulation techniques such as pulse width modulation (PWM) scheme, a primary objective is to calculate the duty cycles for the converter switches that create the desired low frequency target voltage or current output.

The secondary objective is to determine the most effective way of arranging the switching processes to minimize unwanted harmonic distortion, switching losses, and equal switch utilisation. Staircase (square wave) modulation is the most preferable technique for low switching frequency modular multilevel converter. Staircase (fundamental frequency) modulation methods can be classified to multilevel selective harmonic elimination and the nearest level modulation (NLM) [9-15]. In selective harmonic elimination methods, switching angles are computed offline and stored in lookup tables, which are then interpolated according to the operating condition. This will required a large memory to save the calculated angles at different modulation index. With high number of voltage levels, this method is impractical due to the increase of switching angles, complexity in the numerical algorithm and slow dynamic response. With very high number of voltage levels, the NLM approximates the voltage reference to the closest voltage level of the converter. Since the number of sub modules, hence the number of voltage levels, increase for HVDC applications, the NLM is the most reasonable modulation technique.

TABLE I. Operation of Proposed Converter for different modes

	+ve current	-ve current	+ve current	-ve current
Topology 1	 $V_o = V_c$ S=0 (OFF), S_x=1 (ON)	 $V_o = V_c$ S=0 (OFF), S_x=1 (ON)	 $V_o = 0$ S=1 (ON), S_x=0 (OFF)	 $V_o = 0$ S=1 (ON), S_x=0 (OFF)
Topology 2	 $V_o = V_c$ S=0 (OFF), S_x=1 (ON), S_m=1 (ON)	 $V_o = V_c$ S=0 (OFF), S_x=1 (ON), S_m=1 (ON)	 $V_o = 0$ S=1 (ON), S_x=0 (OFF), S_m=1 (ON)	 $V_o = 0$ S=1 (ON), S_x=0 (OFF), S_m=1 (ON)

The NLM method is considerably simpler to implement since it on-line compares a reference sine waveform with available square wave (staircase) waveform and switches the available cells appropriately. Equation (7) is used to know the required number of cells to achieve the desired voltage.

$$N_{on} = round\left(\frac{n}{2}\left(V_{ref}+1\right)\right),\ N_{off} = n - N_{on} \tag{7}$$

where, N_{on}, N_{off} are the number of the ON and OFF cells respectively.

Different cell capacitor voltage balancing schemes have been investigated for multilevel converters. There are three main approaches: using an auxiliary balancing circuit, DC offset addition and switching state redundancy. Redundancy of the switching states is used to maintain the capacitor voltage balancing [16-17]. This method is the common reasonable practical strategy for MMC capacitor voltage balancing. Phase voltage redundant states, phase current polarity and knowledge of the capacitor voltages are required to balance the cell capacitors. Based on the capacitor voltage magnitudes and arm current direction, the capacitor voltage balancing algorithm is developed by sorting the upper and lower capacitors according to their voltages and identifies capacitors with maximum and minimum voltages. This balancing technique can be generalized to n+1 level but it is worth noting that the increasing of the number of level will not only increase the number of measurements (6n capacitor voltages) but also the complexity of the balancing algorithm. Also, the power switches are not equally utilized and with different switching frequency.

IV. Comparison

A comparison between the existing MMC (half and full bridge) and the proposed converter is carried out in this section as shown in Table II The comparison is done under same circuit rated conditions for the different converter topologies. It can be seen that the proposed converter with the two different topologies has more switches or diodes than the half bridge MMC (more losses) but less than the full bridge MMC (less cost). The proposed converter is resilience to DC faults as full bridge MMC. In addition, the proposed converter maintains the modularity feature and the extra power electronics devices are clamped to the cell capacitor voltage not such as alternative arm modular multilevel converter, and a hybrid multilevel converter with ac-side cascaded full-bridge cells.

V. Simulation Results

A case study of 35kV, 20 MVA, 21-level MMC based VSC-HVDC is being considered as interconnection between AC system and DC network as shown in Fig. 2a. For simplicity of the analysis and focus on the response of MMC, the DC link voltage is assumed constant (using DC battery), and in real hardware implementation this can be achieved by using another VSC based converter station at the other terminal. The proposed system parameters are shown in Table III. The proposed MMC VSC-HVDC system control structure consists of three control loops. The outer control loop is the active power and reactive power (AC voltage) controller. The second control loop (current controller) regulates the active and reactive current components over the full operating range. The inner control layer represents the modulator and capacitor voltage balancing mechanism that generates the gating signals. Fig. 2b shows the system control block diagram for the MMC converter.

TABLE III. System Paprmeters

Description	Value
DC link voltage	20kV
Active power rating	20 MW
Reactive power rating	10 MVAr
Cell capacitance	20 mF
Arm inductor	2 mH
Number of cells per arm	20
Cell capacitor voltage	1kV
AC system voltage	35 kV
Transformer ratio	35kV/10kV
Switching frequency	50 Hz

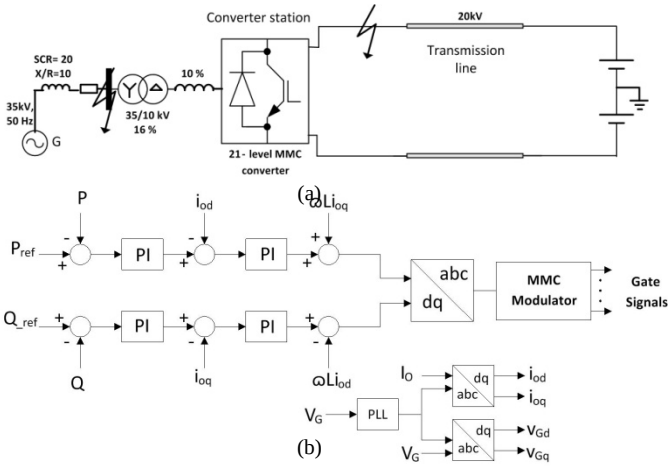


Fig. 2. MMC VSC-HVDC system: (a) system structure and (b) control block diagram

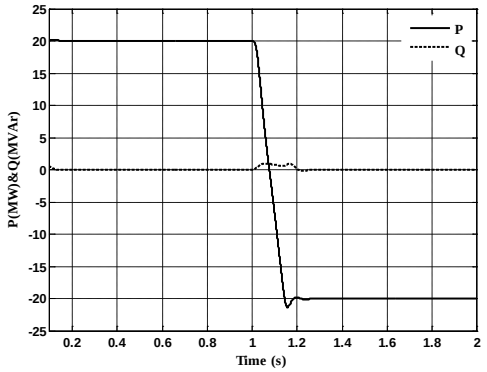
TABLE II. Modular multilevel converter topologies comparison

For n-level	MMC topologies			
	Topology 1	Topology 2	Modular (half bridge)	Modular (Full bridge)
IGBT/phase	4(n-1)	6(n-1)	4(n-1)	8(n-1)
Diode/phase	10(n-1)	6(n-1)	4(n-1)	8(n-1)
Gate drivers/phase	4(n-1)	6(n-1)	4(n-1)	8(n-1)
Switching loss	Medium	Medium	Low	High
Conduction loss	Medium	Medium	Low	High
DC fault	Excellent	Excellent	Poor	Excellent

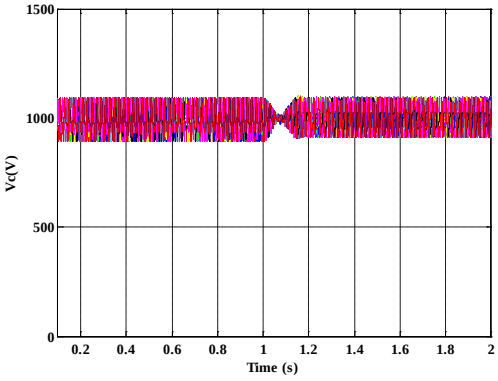
This section provides different simulation results to demonstrate the potential superiority of the proposed converter (topology 1).

A. Steady state and reversal power operation

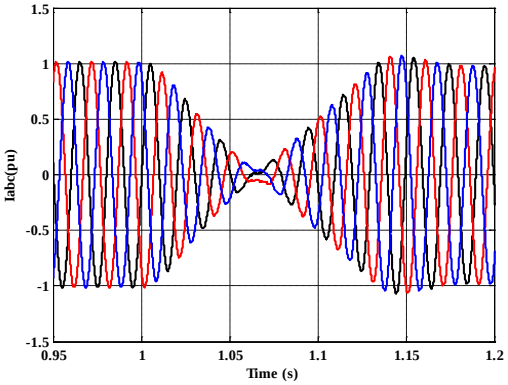
To demonstrate reversal active power operation of the proposed MMC VSC-HVDC system, MMC converter is commanded to import power from the grid (rectifier mode) at rated active power (20 MW). At time 1s it is commanded to reverse the active power flow in order to export 20 MW into grid (inverter mode), at 10 pu/s. Fig. 3a shows converter active and reactive power exchange with the grid. The converter is able to adjust its active power exchange with the grid with good dynamic response. Fig. 3b shows the 40 cell capacitor voltages of phase 'a', which demonstrates that the voltage stresses across the Half-bridge cell capacitors of MMC converter are controlled to the desired set point during the entire period. The three phase AC converter currents are presented in Fig. 3c. It presents high quality current without AC filters installed with low THD due to the high number of levels.



(a)



(b)

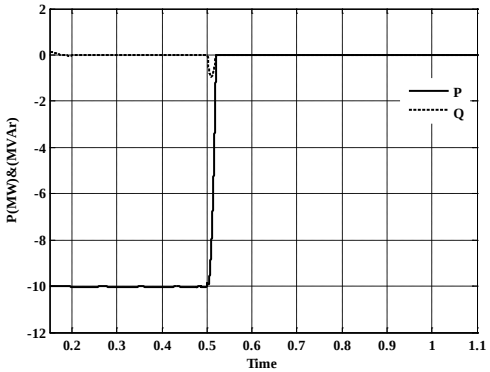


(c)

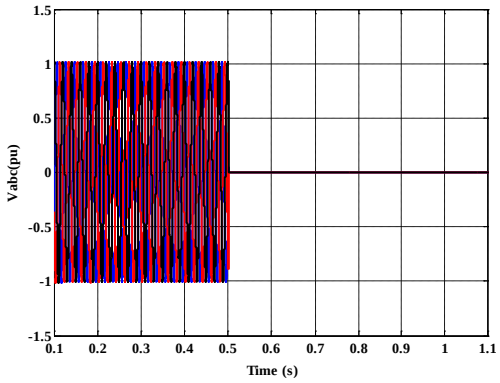
Fig. 3. Steady state operation of MMC based VSC-HVDC system (a) active and reactive power converter exchange with the grid; (b) voltage across 40 cell capacitors of the converter phase 'a' (c) three phase AC current waveforms.

B. AC network fault

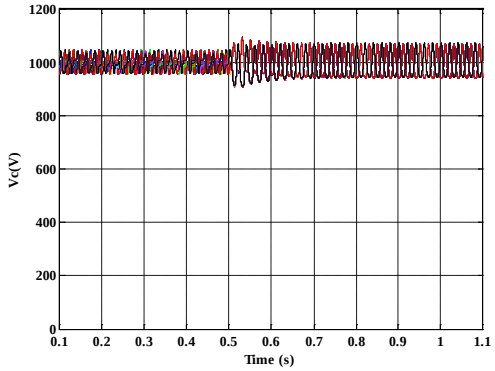
To show the AC fault ride-through capability of the proposed MMC VSC-HVDC system, the test network is subjected to a three-phase fault to ground at the location shown in Fig. 4a. The active power command of the MMC is reduced in proportion to the reduction in the AC voltage magnitude during the fault. This is to minimize the DC link voltage rise because of the trapped energy in the DC side, since power cannot be transferred as the voltage collapses. Fig. 4 displays the results when the test network injects (inverter mode) 0.5 pu (10 MW) into the grid while the system is subjected to a three-phase fault at 0.5s. Fig. 4a shows the converter active and reactive powers exchange with the grid. The MMC converter reduces the injected power to zero as the grid voltage (Fig. 4b) collapses. Fig. 4c shows the voltages across 40 cell capacitors of the MMC converter phase 'a' before and during the fault. It shows that the Half-bridge cell voltage stresses are controlled as the system rides through the AC side fault. The simulation results confirm the capability of the proposed converter to operate in AC faulty networks, independent of its operating point and fault duration.



(a)



(b)

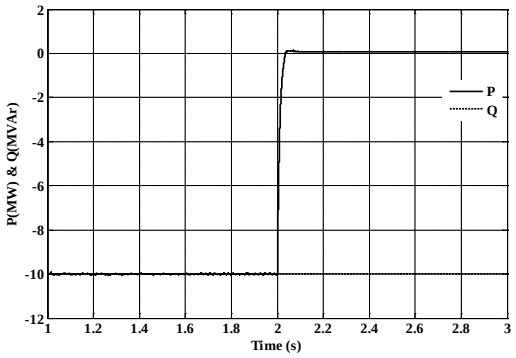


(c)

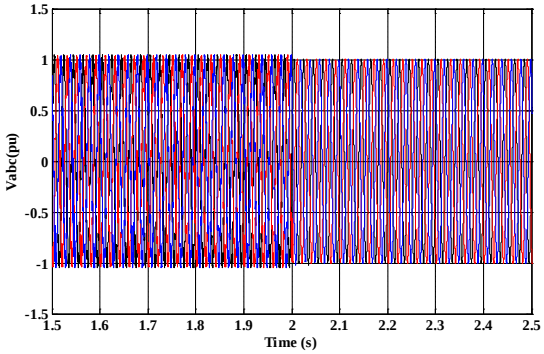
Fig. 4. System waveforms at AC fault: (a) active and reactive power converter exchange with the grid; (b) three phase AC grid voltage waveforms, and (c) voltage across 40 cell capacitors of the converter phase ‘a’.

C. DC network fault

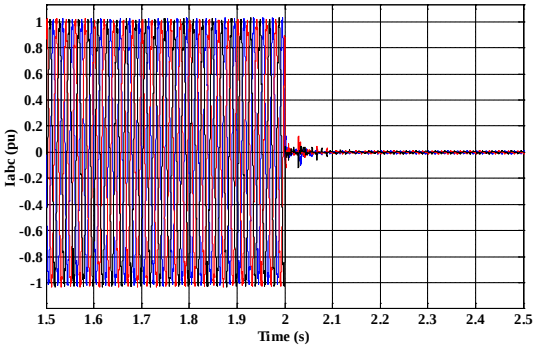
The proposed system is subjected to a solid pole-to-pole DC side fault at the location indicated in Fig. 2a at 2s. During the DC side fault period, inhibiting all converter gate signals to block the converter cells (maintain the capacitor voltages), and due to the existing of embedded diodes, the AC grid current will be blocked to feed the DC side fault until the circuit breaker opens the circuit. Fig. 5a shows the converter active and reactive powers exchange with the grid. It is obvious that the converter changes from inverter to rectifier mode due to the fault. The system is totally controlled as the cells are blocked. Fig. 5b shows the three phase AC grid waveform voltages before and during the fault. The AC voltages are not affected by the DC faults. The three phase current waveforms are shown in Fig. 5c and thanks to the proposed topology; the current is blocked between the AC and DC sides during the DC fault.



(a)



(b)



(c)

Fig. 5. System waveforms at DC fault: (a) active and reactive power converter exchange with the grid, (b) three phase AC grid voltage waveforms, and (c) three phase AC current waveforms.

VI. Conclusion

Two different modified half bridge modular multilevel converter topologies have been proposed. The proposed converter structure control including the converter modulation and capacitor balancing were presented. The proposed converter offers excellent rig through DC fault capability such as full bridge MMC but with less number of switches. This leads to less losses, cost and converter footprint. The voltage across the embedded power electronics devices are clamped to the sub module voltage. Moreover, the proposed converter maintains the modularity compared to other modified conventional converters in literature. A SIMULINK/MATLAB simulation of 21-level MMC based VSC-HVDC has been carried out to verify the converter features and capability during normal and faulty conditions.

References

[1] G.P. Adam, K.H. Ahmed, S.J. Finney, K. Bell, B.W. Williams, "New Breed of Network Fault-Tolerant Voltage-Source-Converter HVDC Transmission System," Power Systems, IEEE Transactions on, Vol. 28, Issue: 1, 2013, pp. 335-346.

[2] G.P. Adam, I. Abdelsalam, K.H. Ahmed, B.W. Williams "Hybrid Multilevel Converter With Cascaded H-bridge Cells for HVDC Applications: Operating Principle and Scalability", IEEE Power Electronics Transactions, 2014, in print.

[3] E. Solas, G. Abad, J.A. Barrena, S. Aurtenetxea, A. Carcar, L. Zajac, "Modular Multilevel Converter With Different Submodule Concepts—Part II: Experimental Validation and Comparison for HVDC Application" Industrial Electronics, IEEE Transactions on, Vol. 60, No. 10, 2013, pp. 4536- 4545.

[4] Qiang Song ; Wenhua Liu ; Xiaoqian Li ; Hong Rao ; Shukai Xu ; Licheng Li "A Steady-State Analysis Method for a Modular Multilevel Converter Power Electronics, IEEE Transactions on, Vol. 28, No. 8, 2013, pp. 3702- 3713.

[5] Minyuan Guan ; Zheng Xu, "Modeling and Control of a Modular Multilevel Converter-Based HVDC System Under Unbalanced Grid Conditions," Power Electronics, IEEE Transactions on, Vol. 27, No. 12, 2012, pp. 4858- 4867.

[6] J. Háfner and B. Jacobson, "Proactive hybrid HVDC breakers-A key innovation for reliable HVDC grids," in *Proc. Cigre Conf.*, Bologna, Italy, Sep. 13-15, 2011, pp. 1–8.

[7] G.P Adam, K.H Ahmed, N.K Singh, S.J Finney, and B.W Williams, 'A Hybrid Multilevel Converter for Medium and High Voltage Applications' IEEE PowerTech, June 2011, pp. 1 – 6.

[8] B. Jaconson et al. , "vsc-hvdc transmission with cascaded two-level converters," in Proc. Cigre Conf., Paris, France, 2010, pp. 1–8.

[9] D. Ahmadi, Z. Ke, L. Cong, H. Yi, and W. Jin, "A Universal Selective Harmonic Elimination Method for High-Power Inverters," IEEE Transactions on Power Electronics, vol. 26, pp. 2743-2752, 2011.

[10] K. Ilves, A. Antonopoulos, S. Norrga, H-P Nee, "A New Modulation Method for the Modular Multilevel Converter Allowing Fundamental Switching Frequency," Power Electronics, IEEE Transactions on, Vol. 27, No. 8, 2012 , pp. 3482- 3494.

[11] G.S. Konstantinou, M.S. Dahidah, V.G. Agelidis, V.G. "Solution trajectories for selective harmonic elimination pulse-width modulation for seven-level waveforms: analysis and implementation," Power Electronics, IET, Vol. 5, Issue: 1, 2012, pp. 22-30.

[12] G. Konstantinou, M. Ciobotaru, V. Agelidis, "Selective harmonic elimination pulse-width modulation of modular multilevel converters," Power Electronics, IET, Vol. 6, Issue: 1, 2013 , pp. 96-107.

[13] Tu Qingrui, Xu Zheng "Impact of Sampling Frequency on Harmonic Distortion for Modular Multilevel Converter," Power Delivery, IEEE Transactions on, vol.26, no.1, Jan. 2011, pp.298-306.

[14] Gum Tae Son ; Hee-Jin Lee ; Tae Sik Nam ; Yong-Ho Chung ; Uk-Hwa Lee ; Seung-Taek Baek ; Kyeon Hur ; Jung-Wook Park "Design and Control of a Modular Multilevel HVDC Converter With Redundant Power Modules for Non-interruptible Energy Transfer," Power Delivery, IEEE Transactions on , Vol. 27, Issue: 3, 2012, pp. 1611-1619.

[15] J. Peralta, H. Saad, S. Dennetire, J. Mahseredjian and S. Nguefeu, "Detailed and averaged models for a 401-level MMC-HVDC system", IEEE Trans. on Power Delivery, vol. 27, no. 3, pp. 1501-1508, July, 2012.

[16] Y. Zhang, et al., "Analysis of modular multilevel converter capacitor voltage balancing based on phase voltage redundant states," IET Power Electronics, volume 5, 2012, pp. 726-738.

[17] D. Fujin, C. Zhe "A Control Method for Voltage Balancing in Modular Multilevel Converters," IEEE Trans. Power Electronics, volume 29, 2014, pp. 66-76.