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Modular Multilevel Converter Based LCL DC/DC Converter for High Power DC Transmission Grids

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***Abstract*—This paper presents a modular multilevel converter (MMC) based DC/DC converter with LCL inner circuit for HVDC transmission and DC grids. Three main design challenges are addressed. The first challenge is the use of MMCs with higher operating frequency compared to common transformer-based DC/DC converters where MMC operating frequency is limited to a few hundred hertz due to core losses. The second issue is the DC fault response. With the LCL circuit, the steady state fault current is limited to a low magnitude which is tolerable by MMC semiconductors. Mechanical DC circuit breakers can therefore be used to interrupt fault current for permanent faults and extra sub-module bypass thyristors are not necessary to protect antiparallel diodes. Thirdly, a novel controller structure is introduced with multiple coordinate frames ensuring zero local reactive power at both bridges in the whole load range. The proposed controller structure is also expandable to a DC hub with multiple ports. Detailed simulations using PSCAD/EMTDC are performed to verify the aforementioned design solutions in normal and fault conditions.**

Keywords— DC grids, LCL DC/DC converter, Modular Multilevel Converter (MMC), Nearest Level Modulation (NLM).

I. INTRODUCTION

DC grids are widely under investigation both at governmental and research levels [1]. With voltage source converter (VSC) based HVDC, most existing links worldwide are point-to-point. There would be significant operational and cost benefit if these lines could be interconnected or tapped on DC side, hence creating multi-terminal DC networks. However, many technical challenges face the implementation of meshed DC grids. Major problems include lack of appropriate DC circuit breakers, power flow control difficulty in meshed grids and interconnecting DC transmission lines with different DC voltages [2]. It has been shown recently that some high power DC/DC converters provide promising solutions for these problems [3-5].

In [3], a megawatt-size thyristor-based DC/DC converter has been proposed. This converter is capable of achieving moderate stepping ratio with inherent fault isolation characteristics. However, it suffers from low switch utilization, low efficiency at high stepping ratio, uncontrollable reactive power and variable frequency control. An IGBT-based DC/DC converter utilizing two VSC converters and a LCL circuit was proposed in [4,5]. It overcomes the drawbacks of the converter in [3] and enables high voltage stepping ratio with fixed frequency AC voltage control. Moreover, with IGBTs, higher frequency is possible compared to thyristors leading to an overall reduction in passive elements footprint. This IGBT-based DC/DC converter uses two-level converter topology which uses series IGBT chains to meet high voltage requirements. This needs complex voltage sharing circuitry and controls.

In this paper, the converter in [5] is designed using modular multilevel converter (MMC) rather than the conventional two-level converters. MMCs have been well known at research level for connection with 50/60Hz grids and have been commercially deployed in the Trans Bay project in California. However, their use in DC/DC converters has only been a subject of recent research [6-9]. In [6-8] MMCs are connected front-to-front via an isolating transformer to obtain voltage stepping and galvanic isolation. However, operation is limited to a few hundred hertz (less than 400Hz) to limit transformer magnetic losses. In addition stepping ratios are low to medium [6]. With the proposed LCL converter, high stepping ratios are achievable, the converter is ideally expandable to an unlimited *N*-port DC hub without the need to re-design transformer core and most importantly no magnetics exist as the inductors are air-core based. With the latter property, frequency can be raised to one or two kilohertz enabling reduction in passive circuit footprint. This becomes a major advantage especially in offshore systems.

DC fault management with MMCs has been studied recently in literature [9-11]. In [9], a MMC-based fault-blocking DC/DC converter is proposed but it uses a high number of semiconductors and magnetic elements. MMCs based on half-bridge sub-modules utilize bypass thyristors to protect switches from DC fault overcurrent [10,11]. The proposed LCL-based converter is designed to confine steady state fault current to a value near rated which is tolerable by sub-module anti-parallel diodes. This does not only save using extra bypass thyristors but also means that relatively slow and cheap mechanical DC circuit breakers can be used to interrupt fault current in a few tens of milliseconds.

For the proposed converter, a novel controller is introduced. The new controller approach is expandable to *N*-port DC hub which is a current field of study by the authors. Therefore the DC/DC converter under study here is referred to as a two-port converter that is possibly expandable to multiport hub. The proposed controller uses multiple coordinate frames to regulate power while maintaining zero reactive power for the entire load range to ensure high operating efficiency especially at partial load.

II. DC/DC CONVERTER STRUCTURE

A. Converter Topology

Fig.1(a) shows the topology of the MMC-based LCL DC/DC Converter. It consists of two MMCs powering an inner LCL AC circuit. The MMC utilizes half-bridge sub-modules with two semiconductor switches per sub-module and comprises of two

phases as depicted in Fig. 1(b). This is the minimum number of phases to interface full pole-to-pole DC voltage. It can be extendable to any number of phases to increase reliability and reduce per phase IGBT current rating. With the two-phase structure considered here, there exists two inductors L_i and two capacitors C_i per port, where i denotes the i^{th} port (i=1,2). The i notation is used to keep generic converter representation for future expansion to multiport DC hub (i=1,..,N). Fig.2 shows typical 5-level MMC output voltage waveform per phase obtained using nearest level modulation (NLM).

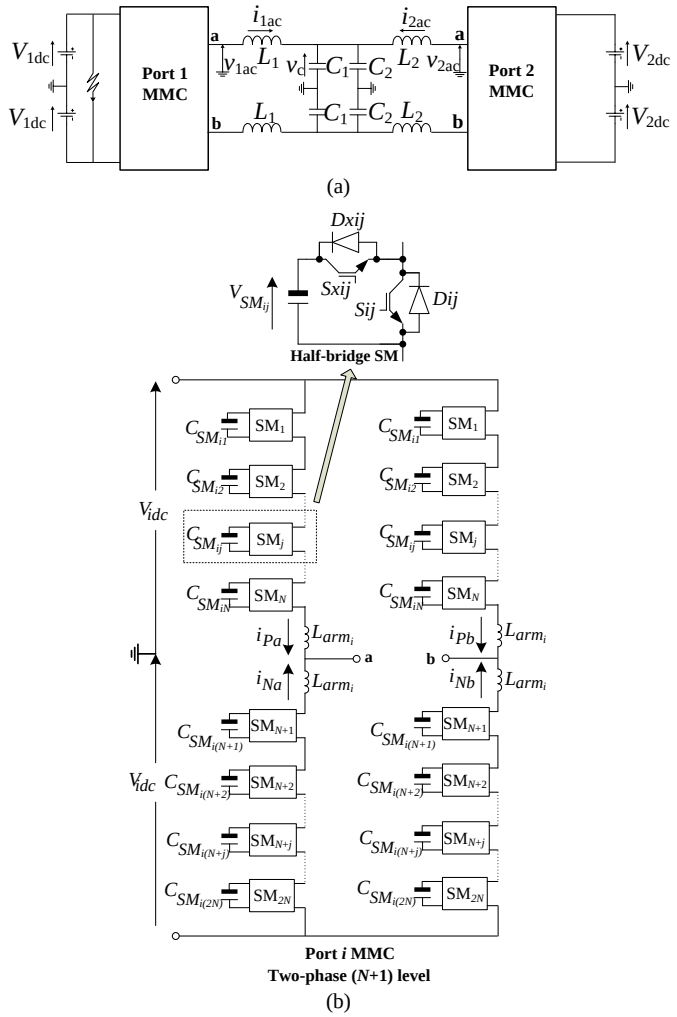


Fig. 1. Topology of MMC-based LCL DC/DC converter.

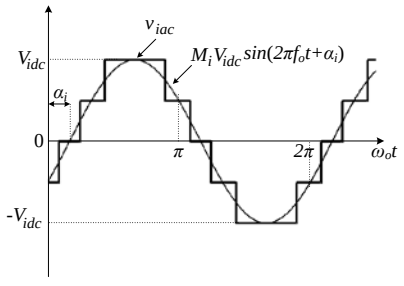


Fig. 2. MMC typical staircase output voltage waveform using NLM.

B. Circuit Equations

Assuming the capacitor voltage v_c to be the reference voltage with zero phase angle, the MMC staircase output voltage can be approximated as a sinusoidal wave

$$v_{iac} = \sqrt{2} V_{iacm} \sin(2\pi f_o t + \alpha_i) \tag{1}$$

where V_{iacm}, f_o, α_i are the RMS magnitude, operating frequency and phase angle of v_{iac}, f_o is fixed. In phasor form,

$$\overline{V_{iac}} = V_{iacm} \angle \alpha_i = V_{iacd} + jV_{iacq} \tag{2}$$

$$\begin{aligned} V_{iacd} &= V_{iacm} \cos\alpha_i = V_{iacm0} M_i \cos\alpha_i \\ V_{iacq} &= V_{iacm} \sin\alpha_i = V_{iacm0} M_i \sin\alpha_i \end{aligned} \tag{3}$$

where V_{iacm0} is the maximum value of V_{iacm} generated by one phase of the MMC $V_{iacm0} = V_{idc}/\sqrt{2}$ and M_i is the modulation index generated by the controller. In dq frame, M_i can be represented as

$$\begin{aligned} M_{id} &= M_i \cos\alpha_i \\ M_{iq} &= M_i \sin\alpha_i \end{aligned} \tag{4}$$

Steady state phasor equations for the LCL circuit are

$$j\omega_o L_i \overline{I_{iac}} = \overline{V_{iac}} - \overline{V_c} \tag{5}$$

$$j\omega_o \overline{V_c} \left(C_1 + C_2\right) = I_{1ac} + I_{2ac} \tag{6}$$

where $\omega_o = 2\pi f_o$. Capacitor C_i voltage is given by

$$\overline{V_c} = V_{cd} + jV_{cq} = V_{cd} = V_c \tag{7}$$

where V_{cq}=0 since coordinate frame is aligned with capacitor voltage. V_c is the RMS AC voltage magnitude of the capacitor voltage v_c. From (5), inductor L_i current is

$$\overline{I_{iac}} = \frac{\overline{V_{iac}} - \overline{V_c}}{j\omega_o L_i} \tag{8}$$

$$I_{iacd} + jI_{iacq} = \frac{V_{iacq}}{\omega_o L_i} + j\frac{V_c - V_{iacd}}{\omega_o L_i} \tag{9}$$

C. LCL Circuit Design

Inductance L_i and capacitance C_i are designed such that zero reactive power is drawn at both MMCs at rated power. Hence equations for active and reactive power are necessary for the design. The per phase complex power S_i at each port is

$$\begin{aligned} S_i &= (V_{iacd} + jV_{iacq})(I_{iacd} - jI_{iacq}) \\ &= (V_{iacd} I_{iacd} + V_{iacq} I_{iacq}) + j(V_{iacq} I_{iacd} - V_{iacd} I_{iacq}) \\ &= P_i + jQ_i \end{aligned} \tag{10}$$

Active and reactive powers constitute the real and imaginery parts of (10) respectively. Substituting by (3), (4) and (9) into (10) yields

$$P_i = \frac{M_{iq} V_{iacm0} V_c}{\omega_o L_i} \tag{11}$$

$$Q_i = \frac{\left(M_{id}^{\ 2} + M_{iq}^{\ 2}\right) V_{iacm0}^{\ 2} - M_{id} V_{iacm0} V_c}{\omega_o L_i} \tag{12}$$

Equating Q_i=0 in (12) and solving simultaneously with (11) yields the value of L_i

$$L_i = \frac{V_{iacm0} \sqrt{V_{cr}^{\ 2} - V_{iacm0}^{\ 2}}}{\omega_o P_{ir}} \tag{13}$$

where V_{cr} is the rated value of V_c and P_{ir} is the rated converter power. The capacitor per phase (C_i) is designed to compensate the reactive current generated by L_i at rated power

$$\omega_o V_{cr} C_i = I_{iacq} = \frac{V_{cr} - V_{iacd}}{\omega_o L_i}$$
$$C_i = \frac{V_{cr} - M_{id} V_{iacm0}}{\omega_o^2 V_{cr} L_i} \quad (14)$$

Using the value of L_i in (13) and solving simultaneously with equating Q_i=0 in (12) yields

$$C_i = \frac{1}{\omega_o V_{cr}^2} \frac{P_{ir}\sqrt{V_{cr}^2 - V_{iacm0}^2}}{V_{iacm0}} \quad (15)$$

LCL circuit design is detailed in [12]. Equations (13) and (15) show that rated capacitor voltage V_{cr} needs to be selected higher than both ports maximum AC output voltage to hold the mathematical relation true.

D. MMC inductance and capacitance selection

According to [13], MMC sub-module capacitance C_{SM} for port *i* can be calculated using

$$C_{SM} = \frac{EP.S_i}{p.N.V_{SM}^2} \quad (16)$$

where *EP* is the energy-power ratio typically in the range of 10J/kVA to 50J/kVA, S_i is rated apparent power, *p* is the port converter number of phases, *N* is the number of sub-modules per MMC arm and V_{SM} is nominal sub-module capacitor voltage. Minimum arm inductance L_{arm} necessary to eliminate a certain even harmonic *h* in MMC circulating current is given by [13],

$$L_{arm} \geq \frac{N}{\omega_o^2 C_{SM}} \frac{2\left(h^2-1\right) + M_i^2 h^2}{8h^2\left(h^2-1\right)} \quad (17)$$

III. DC/DC Converter Control

LCL DC/DC converter control in [4] is based on one port controlling power and the other acting as a balancing port. Control structure is not the same at both ports. In this section a new control strategy is proposed which ensures both ports have identical controls providing structural symmetry. This is particularly useful in case of possible expansion of the converter to multiport structure [12] or in preventing operation failure in case of loss of phase in a multi-phase converter [14]. Fig. 3 shows the overall structure of the proposed converter controls.

A. Power Controller

Local active power P_i at each port can be controlled directly using *q*-axis modulation index M_{iq} as shown by (11). In order to have a reference coordinate frame for control, central capacitor voltage is controlled such that V_{cq}^*=0. Separating (6) into *dq* components, a relation for V_{cq} can be obtained

$$-\omega_o V_{cq}\left(C_1 + C_2\right) = \frac{V_{1acq} - V_{cq}}{\omega_o L_1} + \frac{V_{2acq} - V_{cq}}{\omega_o L_2} \quad (18)$$

Rearranging (18) and applying definitions of V_{iacd} and V_{iacq} in (3) and (4) yields

$$V_{cq}\left(\frac{1}{\omega_o L_1} + \frac{1}{\omega_o L_2} - \omega_o C_1 - \omega_o C_2\right) = \frac{M_{1q} V_{1acm0}}{\omega_o L_1} + \frac{M_{2q} V_{2acm0}}{\omega_o L_2} \quad (19)$$

Equation (19) shows that in order to control V_{cq}, it is necessary to control M_{iq} at either or both ports. Therefore, at each converter port, there exists an outer control loop for power P_i control in addition to another loop in parallel controlling V_{cq}=0. Both loops contribute towards regulating M_{iq}. From (9), currents I_{iacd} and I_{iacq} are controlled using M_{iq} and M_{id} respectively. Therefore, the power control loop has an inner loop to regulate I_{iacd} using M_{iq}. The controller is also designed to operate the converter at zero reactive power in the entire load range. This ensures high efficiency especially at partial load. To control local reactive power at each port to zero, AC voltage V_{iac} and AC current I_{iac} need to be in phase. This is illustrated by the phasor diagram in Fig.4. To facilitate this, a new coordinate frame is used for each port which is aligned with its generated AC voltage V_{iac}. The *q*-component of the AC current I_{iac} in this new frame is controlled to zero to ensure zero local reactive current. The main coordinate frame is denoted by angle θ (θ=0 aligned with central capacitor voltage) and the new local frames at each port are denoted by δ_i such that

$$\delta_i = \theta + \theta_i \quad (20)$$

where θ_i is the angle of the port AC voltage V_{iac}. The *q*-component of I_{iac} in the new frame is denoted by $I_{iacq\_\delta i}$ and is regulated using M_{id} according to (9). The overall structure of the power controller is illustrated in Fig.5. It is worth noting that this control structure is identical at each port, hence more ports can be added and the whole converter is readily expandable to a multiport DC hub. However, with two ports, power transferred from one port is essentially the same as that received by the other; therefore, capacitor voltage can be reduced at partial load to enable zero reactive power. On the contrary, with multiports, one port can be operating at rated power and other ports can be at rated or partial power. This means that capacitor voltage needs to be constant at all times at rated value to enable any port to achieve full power as locally required.

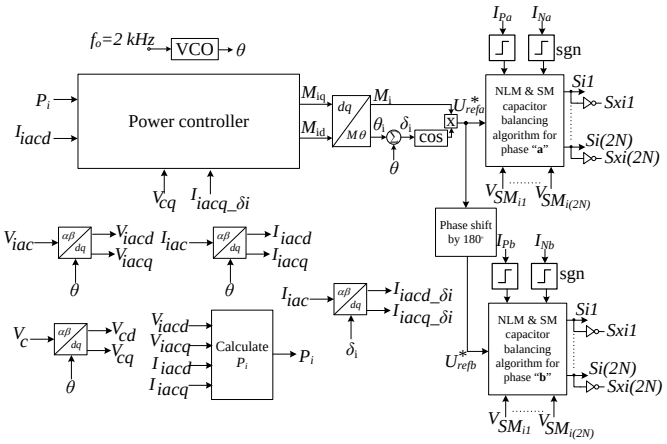


Fig. 3. Overall control structure for port *i*.

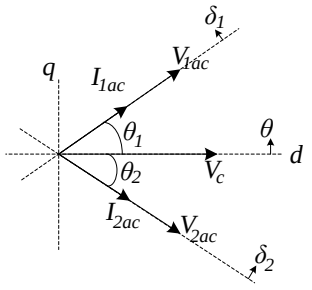


Fig. 4. DC/DC converter phasor diagram.

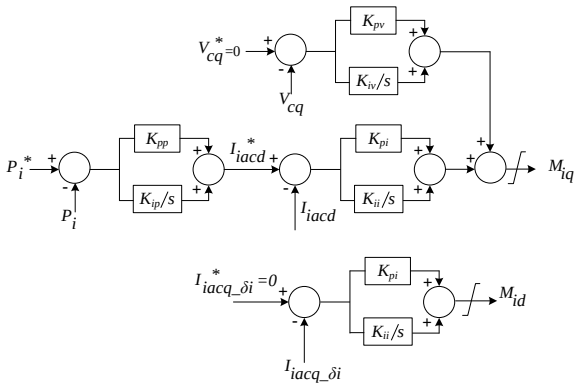


Fig. 5. Structure of the power controller for port *i*.

B. NLM and Sub-module Capacitor Voltage Balancing with Fundamental Frequency Swicthing

The sinusoidal reference voltage U_{refk}^* for each MMC phase leg (k=a,b) is constructed from controller. This is the input to the NLM and capacitor voltage balancing algorithm. The value of the reference signal U_{refk}^* is rounded to the nearest level, hence determining the number of sub-modules to be switched on in each MMC arm. It is the direction of arm currents together with sub-module voltage sorting which determine which sub-modules to be fired/bypassed to maintain capacitor voltage balance. The balancing technique implemented is outlined in [15] but using NLM rather than PWM to achieve IGBT fundamental frequency switching. This gives minimal IGBT switching instants (one pulse per fundamental cycle) and hence reduces switching losses.

IV. SIMULATIONS

PSCAD/EMTDC is used to perform detailed simulations on a 5-level 2-phase 30kW MMC-based LCL DC/DC converter which are the ratings of the current experimental prototype under construction. The converter is operating at f_o=2kHz. This frequency is selected as the highest possible value that would reduce passive elements footprint/mass while ensuring high converter efficiency. Per unit system is used in controls by referring all voltages, currents and powers to rated values at each port. Table I and II show test system parameters.

A. Zero reactive power (full & partial load) and power reversal

The DC/DC converter is simulated as follows:

- **From t=0.0s to t=1.0s**, operation is at rated power, i.e. P_1^*=1.0 pu and P_2^*=-1.0 pu (step down mode).
- **At t=1.0s**, a step full power reversal is performed to step up mode.
- **At t=2.0s**, a step full power reversal is performed again.
- **At t=3.0s**, a step power order is performed from full to partial power, i.e. P_1^*=0.25pu and P_2^*=-0.25 pu.

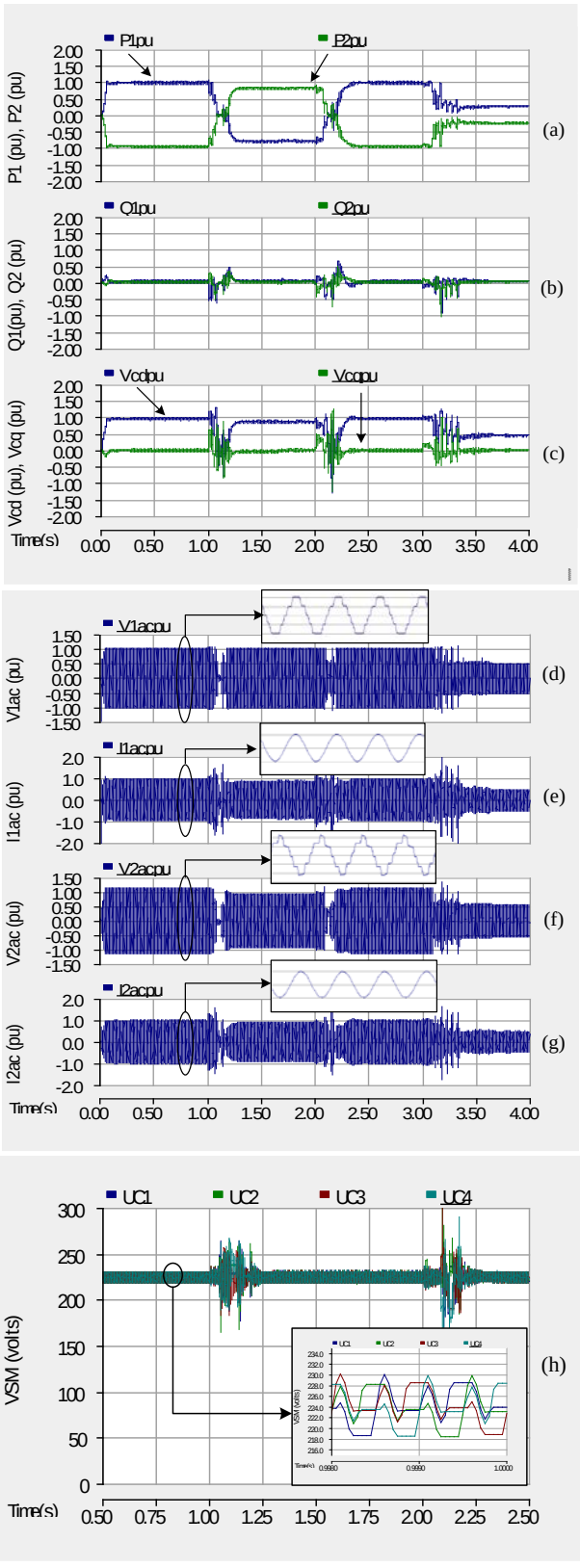
Results are depicted in Fig. 6.

TABLE I. LCL DC/DC CONVERTER PARAMETERS

	P_{ir} (kW)	V_{idc} (V)	V_{cr} (V)	L_i (µH)	C_i (µF)	C_{SMi} (µF)	L_{armi} (µH)	V_{SMi} (V)
Port 1	30	450	552	657	6.67	320	75	225
Port 2	30	100	552	175	35	4060	5.12	50

TABLE II. CONTROL PARAMETERS

Parameter	K_{pv}	K_{iv}	K_{pp}	K_{ip}	K_{pi}	K_{ii}
Value	0.0001	50	0.0001	10	0.0001	20



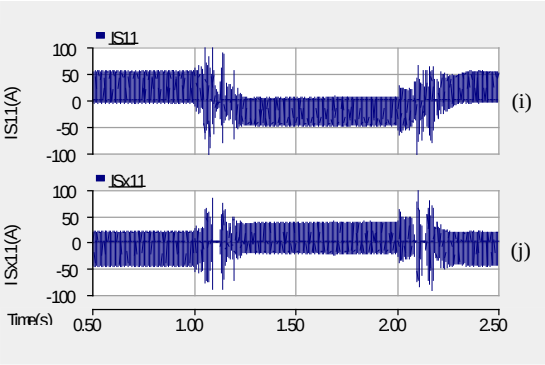


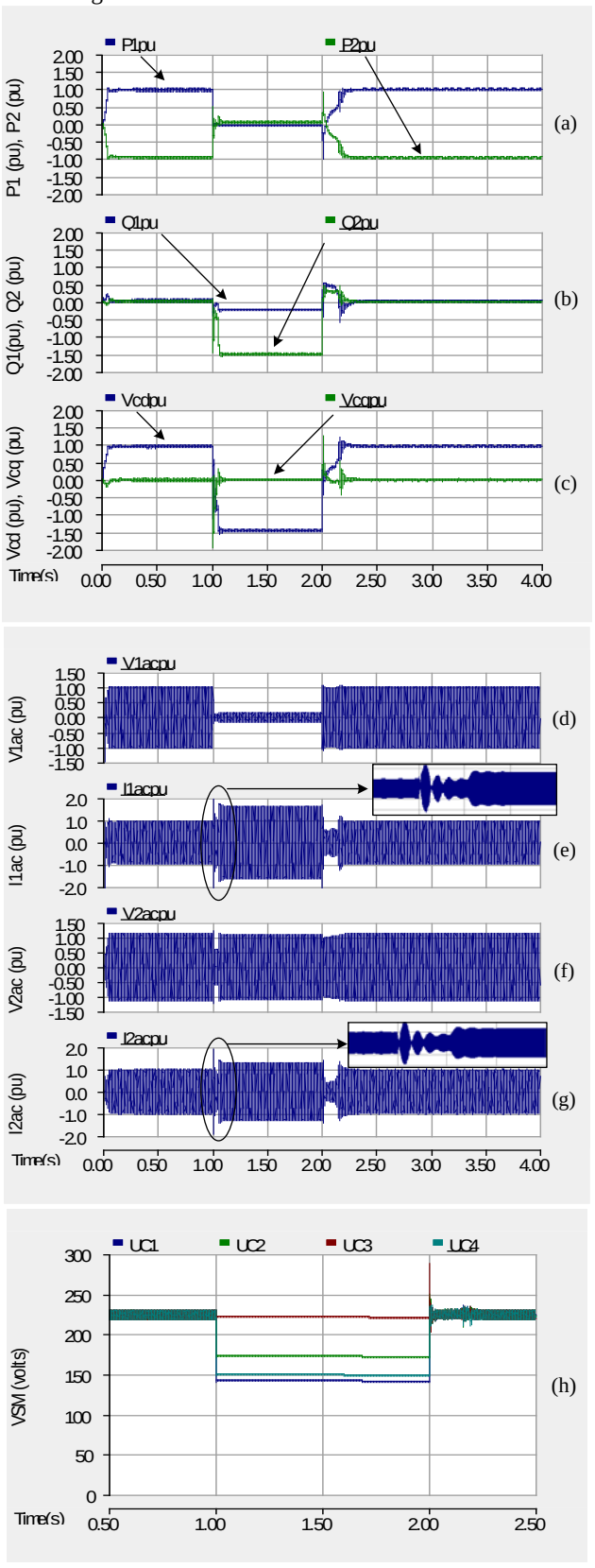
Fig. 6. Results for full/partial power and power reversal (a) Active power (b) Reactive power (c) AC capacitor voltages (d) Port 1 AC voltage (e) Port 1 AC current (f) Port 2 AC voltage (g) Port 2 AC current (h) Port 1 sub-module capcitor voltages (i) Port 1 switch S11 current (j) Port 1 switch Sx11 currrent.

Active power P_i follows reference as shown in Fig. 6(a) satisfying power reversal from step down to step up modes and vice versa in addition to partial load operation at 0.25pu. At full power in steady state, Fig. 6(b) shows reactive power consumption is zero which confirms the L_i and C_i design in (13) and (15). At partial load ($t \geq 3.0s$), zero reactive power is still achieved at both ports thanks to the proposed controller. Fig. 6(c) shows capacitor voltage V_{cq} regulated to 0.0 pu and V_{cd} is varied to maintain zero local reactive power at the ports. At rated power V_{cd} is at rated value (1.0pu), whereas it is reduced to 0.5pu at partial load.

Fig. 6(d)-(g) show AC voltages and currents of the LCL circuit oscillating at 2 kHz fundamental frequency. Closer views of the voltages V_{1ac} and V_{2ac} show 5 level staircase waveforms obtained from the MMCs. At power reversal instants (t=1.0s and t=2.0s), the controller reduces voltage magnitudes to enable gradual power reduction before reversing. With partial load, AC voltages at both ports are reduced to 0.5pu. Currents I_{1ac} and I_{2ac} reduce to 0.5 pu for partial power operation. Fig. 6(h) shows a sample of port 1 MMC sub-module capacitor voltages during the power reversal instants. Capacitor voltages are well balanced during all stages of operation with steady state voltage ripple of 6%. Fig. 6(i) and (j) show sub-module switch currents. Average current direction changes at t=1.0s and t=2.0s due to power reversal. In switch S11, majority of conduction changes from IGBT to its anti-parallel diode D11 after reversal, and the opposite operation occurs in switch Sx11. Peak transient currents during reversal are less than to 2.0pu. Most semiconductors can tolerate such transient overcurrent and no excessive switch overrating is necessary.

B. DC fault study

A pole-to-pole DC fault is applied to the high voltage DC side (V_{1dc}=0). The DC/DC converter is initially operating at full power in step down mode ($t \leq 1.0s$). A temporary DC fault is applied between t=1.0s and t=2.0s. During the fault, all port 1 IGBTs are tripped. The protection logic implemented utilizes overcurrent and undervoltage protection at the DC side so that the first of the two to reach a pre-set threshold triggers fault flag that trips IGBTs. This not only minimizes sub-module capacitor discharge to enable restart of power transmission after temporary fault, but also protects IGBTs from high transient discharge currents. To allow for practical circuit delays (including delays from sensing, hardware propagation time, microcontroller …etc), the trip signal is delayed by a pre-set value of 0.1ms in simulation. Results are shown in Fig. 7.



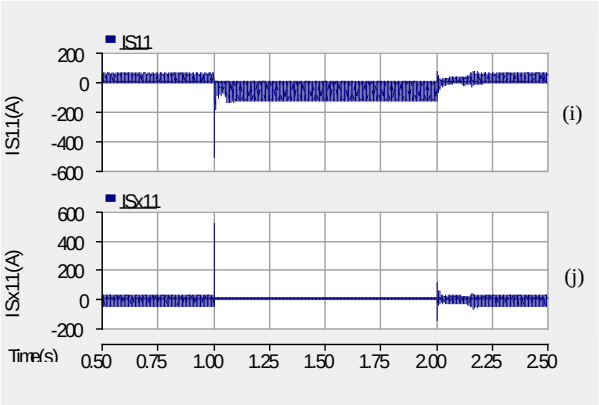


Fig. 7. Results for DC fault at port 1 (a) Active power (b) Reactive power (c) AC capacitor voltages voltages (d) Port 1 AC voltage (e) Port 1 AC current (f) Port 2 AC voltage (g) Port 2 AC current (h) Port 1 sub-module capcitor voltages (i) Port 1 switch S11 current (j) Port 1 switch Sx11 currrent.

Fig. 7(a) and (b) show that power drops to zero during the fault, with port 2 supplying only reactive power to the LCL circuit. Fig. 7(c) shows the V_{cq}=0 during the fault whereas V_{cd} becomes -1.5pu since port 2 is supporting the faulted port with reactive power. For this reason, using this control structure in DC/DC converter operation, the capacitor needs to be designed for 1.5 pu of its rated voltage. This is not the case in a multiport DC hub where capacitor voltage is controlled to rated value all the time. The LCL circuit is designed to provide converter fault tolerant operation. This is clear in Fig. 7(e) and (g) where steady state AC current at the faulted port side (I_{1ac}) is limited to 1.5pu and to 1.2pu at the unfaulted port. Semiconductors can be easily selected to tolerate such current. Normally MMC switches in HVDC converters will have antiparallel thyristors but the above study shows that MMC with LCL DC/DC may not need antiparallel thyristors.

In case the fault is permanent, a mechanical DC circuit breaker (CB) can be used to isolate the fault at the unfaulted port side. These are relatively cheaper and simpler than semiconductor CBs which are yet not available at commercial scale. Fig. 7(h) shows sub-module capacitor voltages which discharge partially due to the 0.1ms pre-set delay in tripping the IGBTs when the fault occurs at t=1.0s. The amount of discharge in each capacitor is dependent on the conduction time of switch Sx in series with the sub-module capacitor during the 0.1ms period. This phenomenon is apparent in Fig. 7(j) showing switch Sx11 current. Due to switch tripping, its current falls to zero during the fault period after reaching a peak discharge transient current of 6.5pu (500A) in 0.1ms duration. Fig. 7(i) shows how switch S11 current reverses during fault since power from port 2 is feeding the fault. D11 conducts the 1.5pu steady state fault current.

V. Conclusion

This paper presented a MMC based LCL DC/DC converter that is applicable for future DC transmission grids. Three main challenges were addressed. The first challenge is the MMC high operating frequency. To reduce the resulting IGBT switching losses, capacitor balancing with fundamental frequency switching has been applied with NLM. Secondly the issue of steady state fault current was studied. Fault current is confined to a maximum of 1.5pu by the LCL circuit which means load-rated (not fault-rated) semiconductors can be used. In addition this saves using extra bypass thyristors at sub-modules and most importantly means that commercially available mechanical DC circuit breakers can be used to interrupt fault current in a few tens of milliseconds. Thirdly, a novel controller structure with multiple coordinate frames was presented to ensure zero local reactive power at each port in the entire load range. It is also identical in structure at each port to make expandability to multiport hub feasible. Transient and steady state converter behaviour has been verified using detailed PSCAD simulations.

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